What is claimed is:

1. A semiconductor memory device, comprising:

a memory cell array including a plurality of word lines and a plurality of bit lines to which memory cells are connected;

a row decoder for generating a word line select signal, according to an address signal, to simultaneously select two word lines neighboring each other of the plurality of the word lines;

a column decoder for selecting one of the plurality of the bit lines; and

a plurality of sense amplifiers for sensing data stored at the memory cells selected by the row decoder and the column decoder.

2. The semiconductor memory device as claimed in claim 1, wherein the row decoder decodes only remaining address signals of the address signals except for a lowest address signal to generate the word line select signal, so that the two neighboring word lines are selected at the same time.

3. The semiconductor memory device as claimed in claim 2, wherein the row decoder generates the word line select signal of a number corresponding to a half of the word line and simultaneously selects the two neighboring word lines using one word line select signal.

4. The semiconductor memory device as claimed in claim 1,

wherein the row decoder comprises:

a plurality of inverters for inverting the address signals; and

a plurality of NOR gates for combining the address signals and inverted address signals to generate the word line select signals, wherein the ground voltage is instead applied to input terminals of the NOR gates to which the lowest address signal is inputted,

whereby the lowest address signal is processed as "Don't care" in order to enable the word line select signals twice each time so that the two neighboring word lines are selected at the same time.

5. The semiconductor memory device as claimed in claim 4, wherein the row decoder further comprises a switching means provided at the input terminal of the NOR gate to which the lowest address signal is inputted, for selectively switching either the lowest address signal or the ground voltage to the input terminal of the NOR gate according to a control signal, whereby if the lowest address signal is inputted, only one word line is selected and if the ground voltage is inputted, the two word lines are selected at the same time.

6. The semiconductor memory device as claimed in claim 1, wherein the row decoder comprises:

a plurality of inverters for inverting the address signals; and

a plurality of NAND gates for combining the address signals and inverted address signals to generate the word line select signals, wherein the power supply voltage is instead applied to the input terminals of the NAND

gates to which the lowest address signal is inputted,

whereby the lowest address signal is processed as "Don't care" in order to enable the word line select signals twice each time so that the two neighboring word lines are selected at the same time.

7. The semiconductor memory device as claimed in claim 6, wherein the row decoder further comprises a switching means provided at the input terminal of the NOR gate to which the lowest address signal is inputted, for selectively switching either the lowest address signal or the power supply voltage to the input terminal of the NOR gate according to a control signal, whereby if the lowest address signal is inputted, only one word line is selected and if the ground voltage is inputted, the two word lines are selected at the same time.

8. The semiconductor memory device as claimed in claim 1, wherein one of the two neighboring word lines is a word line to which true cells connected to the bit lines are connected and the other of the word lines is a word line to which complement cells connected to the inverted bit lines are connected.

9. The semiconductor memory device as claimed in claim 8, wherein the true cells are connected to first input terminals of the sense amplifiers through the bit lines and the complement cells are connected to second input terminals of the sense amplifiers through the inverted bit lines,

whereby stored data are read.

10. The semiconductor memory device as claimed in claim 1, wherein the two neighboring word lines are word lines to which only true cells connected to the bit lines are connected, or word lines to which only complement cells connected to inverted bit lines are connected.

11. The semiconductor memory device as claimed in claim 10, wherein the true cells or the complement cells are connected to first input terminals of the sense amplifiers and a reference voltage is applied to second input terminals of the sense amplifiers, whereby stored data are read.

12. A semiconductor memory device, comprising:

a memory cell array including a plurality of word lines, a plurality of bit lines and a plurality of inverted bit lines to which memory cells are connected;

a row decoder for selecting one of the plurality of the word lines;

a column decoder for generating a bit line select signal, according to an address signal, to simultaneously select two bit lines neighboring each other of the plurality of the bit lines, or two inverted bit lines neighboring each other of the plurality of the inverted bit lines; and

a plurality of sense amplifiers for sensing data stored at the memory cells selected by the row decoder and the column decoder,

wherein the two neighboring bit lines and the two neighboring inverted

bit lines are each connected in parallel to different input terminals of the sense amplifiers.

13. The semiconductor memory device as claimed in claim 12, wherein the column decoder decodes only remaining address signals of the address signals except for a lowest address signal to generate the bit line select signal, so that the two neighboring bit lines or the two neighboring inverted bit lines are selected at the same time.

14. The semiconductor memory device as claimed in claim 13, wherein the column decoder generates the bit line select signal of a number corresponding to a half of the bit line and simultaneously selects the two neighboring word lines using one bit line select signal.

15. The semiconductor memory device as claimed in claim 12, wherein the column decoder comprises:

a plurality of inverters for inverting the address signals; and

a plurality of NOR gates for combining the address signals and inverted address signals to generate the bit line select signals, wherein the ground voltage is instead applied to input terminals of the NOR gates to which the lowest address signal is inputted,

whereby the lowest address signal is processed as "Don't care" in order to enable the bit line select signals twice each time so that the two neighboring bit lines are selected at the same time.

16. The semiconductor memory device as claimed in claim 12, wherein the column decoder comprises:

a plurality of inverters for inverting the address signals; and

a plurality of NAND gates for combining the address signals and inverted address signals to generate the bit line select signals, wherein the power supply voltage is instead applied to the input terminals of the NAND gates to which the lowest address signal is inputted,

whereby the lowest address signal is processed as "Don't care" in order to enable the bit line select signals twice each time so that the two neighboring bit lines are selected at the same time.